APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/902,140	07/10/2001	Karl-Eugen Kroell	DE9-2000-0026	7994

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INTERNATIONAL BUSINESS MACHINES CORPORATION
DEPT. 18G
BLDG. 300-482
2070 ROUTE 52
HOPEWELL JUNCTION, NY   12533

EXAMINER
JONES, HUGH M

ART UNIT	PAPER NUMBER
2123	5

DATE MAILED: 09/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

Office Action Summary	Application No. 09/902,140	Applicant(s) Kroell et al.	
	Examiner Hugh Jones	Art Unit 2123	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ___3___ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Sep 8, 2003* _____ .

2a) ☒ This action is **FINAL**.   2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1, 2, 5-8, 13, and 14* _____ is/are pending in the application.

    4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1, 2, 5-8, 13, and 14* _____ is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

    If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☒ All b) ☐ Some* c) ☐ None of:

      1. ☒ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    *See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

    a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____

4) ☐ Interview Summary (PTO-413) Paper No(s). _____

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____

DETAILED ACTION

Introduction

1.   Claims 1-14 of U. S. Application 09/902,140 filed on 07-10-2001, are presented for

examination. Claims 3-4, 9-12 have been cancelled. Claims 1-2, 5-8, 13-14 remain for

consideration and have been finally rejected.

Double Patenting

2.   The nonstatutory double patenting rejection is based on a judicially created doctrine

grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or

improper timewise extension of the "right to exclude" granted by a patent and to prevent possible

harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed.

Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686

F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA

1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

3.   A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to

overcome an actual or provisional rejection based on a nonstatutory double patenting ground

provided the conflicting application or patent is shown to be commonly owned with this

application. See 37 CFR 1.130(b).

4.   Effective January 1, 1994, a registered attorney or agent of record may sign a terminal

disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5.   Claims 1-2, 5-8, 13-14 are rejected under the judicially created doctrine of

obviousness-type double patenting as being unpatentable over claims 1-19 of U.S. Patent

No. 6,442,735 in view of Dangelo et al. (US Patent 5,555,201). Although the conflicting claims

are not identical, they are not patentably distinct from each other for the following reasons. The

patented claims refer to an "object list" in apparent reference to object oriented concepts while

the pending claims do not refer to object classes. Dangelo et al. discloses use of object-oriented

circuit simulation wherein the means for circuit simulation may include one or more general

purpose computers interfaced to the ECAD system's computer, one or more hardware simulators

interfaced to the ECAD system's computer, or any combination of these. The user interacts with

the ECAD system through the use of an object-oriented user interface, whereby the user may

create, select, move, modify and delete objects on the display screen, where objects may

represent circuit components, wires, commands, text values, or any other visual representation of

data. The graphical and software techniques of interacting with a user on such an object-oriented

user interface are well known to those skilled in the art and need not be elaborated upon in this

discussion. It would have been obvious to one of ordinary skill in the art at the time of the

invention to modify the teachings of Joshi et al. with the teachings of Dangeo et al. because of

the ease of use of such techniques - see Dangelo et al. (Col. 3, lines 45-56), "Typically, the form

of user interaction with the schematic editor is an object-oriented screen display whereby the user

thereof may manipulate objects on the screen through the use of a pointing device. A pointing

device is any device through the use of which a user may "point" to and identify objects on a

display screen. Such object-oriented interfaces are well known to those skilled in the art. One

example of such and interface is the Macintosh Finder for the Apple Macintosh computer, both

produced by Apple Computer, Inc."

Claim Interpretations

6.   The broadest reasonable interpretation has been given to the claims. The Examiner

interprets that static error corresponds to the DC-simulation and that dynamic error corresponds

to the transient analysis. The Examiner further interprets that the transient analysis is also carried

out on the same exact circuit and with the same conditions.

Claim Rejections - 35 USC § 102

7.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

8.   A person shall be entitled to a patent unless -

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public
> use or on sale in this country, more than one year prior to the date of application for patent in the United
> States.
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before
> the invention by the applicant for patent, except that an international application filed under the treaty
> defined in section 351(a) shall have the effect under this subsection of a national application published
> under section 122(b) only if the international application designating the United States was published under
> Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by
> the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes
> of this subsection based on the filing of an international application filed under the treaty defined in section
> 351(a).

9.   Claims 1, 5, 7, 13 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Wong (US Patent 4,918,643) or Wong et al. (IEEE - 1997).

10.   Wong (US Patent 4,918,643) discloses a method of accelerating the pace at which circuit simulators are able to converge to a steady state solution of a periodic piecewise-linear system or periodically driven piecewise-linear system transforms the problem into finding the solution of a nonlinear function in terms of a state vector, which is then solved by a truncated power series such as the Newton-Raphson iterative procedure. Usage of this method requires the determination of system sensitivity with respect to the state vector. This system sensitivity is determined by solving for the sensitivity of the state vector at the exit of each subinterval of the periodic cycle with respect to the state vector at the entry of the same subinterval. This sensitivity is accurately resolved by considering the sensitivity of the time duration spent in this subinterval with respect to the state vector at the entry of the same subinterval. The sensitivity of time duration is factored into the computation process by computing a subinterval Jacobian matrix for each subinterval. This subinterval Jacobian matrix is computed by adding a subinterval correction matrix to a subinterval state transition matrix to account for changes in subinterval time duration. The cyclic Jacobian matrix for the entire periodic cycle is computed and utizlied in an iteration procedure to adjust a value of the initial state vector. *In particular, Wong discloses DC analysis with error detection and correction - see fig. 2, 3-4, 13; col. 2, lines 7-33; col. 3, line 23 to col. 5, line 14; col. 11-12.*

11.   Wong et al. (IEEE - 1997) discloses "*Accelerated steady-state analysis technique for*

PWM DC/DC switching regulators." Wong et al. further disclose an iterative technique for

steady-state analysis of PWM DC/DC switching regulators. The algorithm consists of two

iteration loops. The first one is to iterate the steady-state network waveforms at a presumed duty

cycle while the second one is to iterate the steady-state duty cycle of the pulse-width modulator

output. The circuit waveforms are obtained by a stepwise time domain simulation method, which

is based on using stepwise quadratic formulations of the circuit stale variables with progressive

analysis of switches' state. *In particular, Wong et al. discloses DC analysis with error detection*

and correction - see fig. 2-3 and corresponding text.

12.   Claims 1-2, 5-8, 13-14 are rejected under 35 U.S.C. 102(e) as being clearly

anticipated by Joshi et al. (US Patent 6,442,735).

13.   Joshi et al. disclose a computer program product method of circuit design of a multiple

input circuit, macro or chip, especially for silicon on insulator (SOI) circuits. For a multiple input

circuit, an object list of items corresponding to circuit devices is created. The items model local

effects on corresponding circuit elements. *The circuit is analyzed using Static or DC analysis to*

provide initial local effects on circuit devices, including body effects and local heat effects. The

initial local effects are passed to the circuit model for transient analysis. The local effects from

checked transient results are checked and updated. The transient response is rerun and the

local effects are updated until the change in local effects is below an upper limit. For added

efficiency, unswitching devices may be eliminated from the iterative analysis and analysis may

be limited to the period when switching occurs. Note figure 2 and corresponding text, including

DC analysis, use of macro and cover models to edit the static error, transient analysis and, again,

use of macro and cover model to edit errors.

Claim Rejections - 35 USC § 103

14.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

15.   The factual inquiries set forth in *Graham v. John Deere Co.*, 148 USPQ 459, that are

applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are

summarized as follows:

   1. Determining the scope and contents of the prior art.

   2. Ascertaining the differences between the prior art and the claims at issue.

   3. Resolving the level of ordinary skill in the pertinent art.

   4. Considering objective evidence present in the application indicating obviousness or

unobviousness.

16.   **Claim 1-2, 5-8, 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over**

Sakamoto in view of Wong (US Patent 4,918,643) or Wong et al. (IEEE - 1997).

17.   Sakamoto discloses: "FIG. 2 is a flowchart illustrating this second prior art. In a step S21,

circuit information is input, and in a step S22, a time Tcal for calculating the eigenvalue is read.

In succeeding steps S23 and S24, a circuit matrix is prepared, and a *DC analysis* is carried

out. *In a step S25, a transient analysis is conducted,* and when the analysis time becomes the

time Tcal, matrix data is written into a magnetic disk. After a series of steps (S31 to S36) for the

transient analysis are completed, a step S26 for processing the eigenvalue display is conducted. In

brief, the matrix data is read out (step S37), and the eigenvalue is calculated on the basis of the

read-out matrix data (step S38). A real-number part and an imaginary-number part of the

calculated eigenvalue are displayed on an X coordinate axis and a Y coordinate axis, respectively

(step S39)."

18.   Thus, Sakamoto discloses a steady-state simulation followed by a transient simulation

(fig. 3 and corresponding text).

19.   Sakamoto does not expressly disclose checking the simulations for errors and then

correcting the errors. Wong or Wong et al. disclose checking simulations to ensure accuracy and

correcting the simulations when the error is deemed significant.

20.   Wong (US Patent 4,918,643) discloses a method of accelerating the pace at which circuit

simulators are able to converge to a steady state solution of a periodic piecewise-linear system or

periodically driven piecewise-linear system transforms the problem into finding the solution of a

nonlinear function in terms of a state vector, which is then solved by a truncated power series

such as the Newton-Raphson iterative procedure. Usage of this method requires the

determination of system sensitivity with respect to the state vector. This system sensitivity is

determined by solving for the sensitivity of the state vector at the exit of each subinterval of the

periodic cycle with respect to the state vector at the entry of the same subinterval. This sensitivity

is accurately resolved by considering the sensitivity of the time duration spent in this subinterval

with respect to the state vector at the entry of the same subinterval. The sensitivity of time

duration is factored into the computation process by computing a subinterval Jacobian matrix for

each subinterval. This subinterval Jacobian matrix is computed by adding a subinterval

correction matrix to a subinterval state transition matrix to account for changes in subinterval

time duration. The cyclic Jacobian matrix for the entire periodic cycle is computed and utizlied in

an iteration procedure to adjust a value of the initial state vector. *In particular, Wong discloses*

DC analysis with error detection and correction - see fig. 2, 3-4, 13; col. 2, lines 7-33; col. 3,

line 23 to col. 5, line 14; col. 11-12.

21.   Wong et al. (IEEE - 1997) discloses *"Accelerated steady-state analysis technique for*

PWM DC/DC switching regulators." Wong et al. further disclose an iterative technique for

steady-state analysis of PWM DC/DC switching regulators. The algorithm consists of two

iteration loops. The first one is to iterate the steady-state network waveforms at a presumed duty

cycle while the second one is to iterate the steady-state duty cycle of the pulse-width modulator

output. The circuit waveforms are obtained by a stepwise time domain simulation method, which

is based on using stepwise quadratic formulations of the circuit state variables with progressive

analysis of switches' state. *In particular, Wong et al. discloses DC analysis with error detection and correction - see fig.* 2-3 and corresponding text.

22.   It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Sakamoto with the teachings of Wong or Wong et al. to obtain the claimed invention for the following reasons. Steady-state and transient simulations are not very useful or realistic if they are not accurate.

Response to Arguments - Claim Objections (pg. 5, paper # 4)

23.   Applicant's arguments, filed 9/8/2003, have been fully considered, and are persuasive. The objections are moot and are withdrawn in view of the amendment (paper # 4).

Response to Arguments - 112 Rejections (pg. 5, paper # 4)

24.   Applicant's arguments, filed 9/8/2003, have been fully considered, and are persuasive. The rejections are moot and are withdrawn in view of the amendment (paper # 4).

Response to Arguments - 101 Rejections (pg. 5, paper # 4)

25.   Applicant's arguments, filed 9/8/2003, have been fully considered, and are persuasive. The rejections are withdrawn in view of the amendment (paper # 4).

Response to Arguments - Double Patenting Rejections (pg. 6, paper # 4)

26.   Applicant's arguments, filed 9/8/2003, have been fully considered, but are not persuasive.

27.   In response to applicant's argument relating to Joshi, please see, for example, limitation e

of claim 2.

28.   In response to applicant's argument that the references fail to show certain features of

applicant's invention, it is noted that the features upon which applicant relies (i.e., that Joshi does

not disclose or suggest "performing corrections based on such comparison of conditions prior to

transient analysis") are not recited in the rejected claim(s). Although the claims are interpreted in

light of the specification, limitations from the specification are not read into the claims. See *In re*

Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Response to Arguments - 102 Prior Art Rejections (pp. 6-7, paper # 4)

29.   Applicant's arguments, filed 9/8/2003, have been fully considered, but are not persuasive.

30.   In response to applicant's argument (Applicants have alleged that the arguments against

double patenting apply equally well to anticipation) relating to Joshi, please see the preceding

arguments relating to Joshi in this action.

31.   In response to applicant's argument that the references fail to show certain features of

applicant's invention, it is noted that the features upon which applicant relies (i.e., that Joshi does

not disclose or suggest "performing corrections based on such comparison of conditions prior to

transient analysis") are not recited in the rejected claim(s). Although the claims are interpreted in

light of the specification, limitations from the specification are not read into the claims. See *In re*

Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

32.   In response to applicant's argument relating to Wong ('643 patent), it is noted that the

sections, as indicated by Applicants (page 6, paper # 4) do not appear to disclose the alleged

features as argued by Applicants. In any case the indicated col. 2, refers to "background"

teachings. Applicants are silent with respect to the sections of the patent as directed by the

Examiner. Wong (US Patent 4,918,643) discloses a method of accelerating the pace at which

circuit simulators are able to converge to a steady state solution of a periodic piecewise-linear

system or periodically driven piecewise-linear system transforms the problem into finding the

solution of a nonlinear function in terms of a state vector, which is then solved by a truncated

power series such as the Newton-Raphson iterative procedure. Usage of this method requires the

determination of system sensitivity with respect to the state vector. This system sensitivity is

determined by solving for the sensitivity of the state vector at the exit of each subinterval of the

periodic cycle with respect to the state vector at the entry of the same subinterval. This sensitivity

is accurately resolved by considering the sensitivity of the time duration spent in this subinterval

with respect to the state vector at the entry of the same subinterval. The sensitivity of time

duration is factored into the computation process by computing a subinterval Jacobian matrix for

each subinterval. This subinterval Jacobian matrix is computed by adding a subinterval

correction matrix to a subinterval state transition matrix to account for changes in subinterval

time duration. The cyclic Jacobian matrix for the entire periodic cycle is computed and utizlied in

an iteration procedure to adjust a value of the initial state vector. *In particular, Wong discloses DC analysis with error detection and correction - see fig. 2, 3-4, 13; col. 2, lines 7-33; col. 3, line 23 to col. 5, line 14; col. 11-12.*

33.   In response to arguments relating to Wong (IEEE), Applicants are, again, silent as to the sections of the applied prior art which were indicated in the rejection. *Wong et al. discloses DC analysis with error detection and correction - see fig.* 2-3 and corresponding text. Applicant's arguments do not clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made.

Response to Arguments - 103 Prior Art Rejections (pg. 7, paper # 4)

34.   Applicant's arguments, filed 9/8/2003, have been fully considered, but are not persuasive.

35.   In response to arguments relating to Sakamoto, Applicants are, again, silent as to the sections of the applied prior art which were indicated in the rejection. Applicant's arguments do not clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. Applicants arguments rely on their arguments against the 102 rejections and are not persuasive for the same reasons. Furthermore, in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusion

36.   Applicant's amendment necessitated the new ground(s) of rejection presented in this

Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

37.   A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR

1.136(a) will be calculated from the mailing date of the advisory action. In no event, however,

will the statutory period for reply expire later than SIX MONTHS from the date of this final

action.

38.   Any inquiry concerning this communication or earlier communications from the

examiner should be:

directed to: Dr. Hugh Jones telephone number (703) 305-0023, Monday-Thursday 0830 to
0700   ET, *or* the examiner's supervisor, Kevin Teska, telephone number (703) 305-
9704.   Any inquiry of a general nature or relating to the status of this application should
be   directed to the Group receptionist, telephone number (703) 305-3900.

mailed to: Commissioner of Patents and Trademarks
              Washington, D.C. 20231

or faxed to: (703) 308-9051 (for formal communications intended for entry) *or*
              (703) 308-1396 (for informal or draft communications, please label
"PROPOSED"   or *"DRAFT"*).

Dr. Hugh Jones

Primary Patent Examiner

September 12, 2003